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Docket No.: 057454-0180 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Customer Number: 20277
Toyohiko YOSHIDA	:	Confirmation Number: 5586
Application No.: 09/911,739	:	Group Art Unit: 2183
Filed: July 25, 2001	:	Examiner: Jacob Andrew Petranek

For: DATA PROCESSING DEVICE WITH INSTRUCTION TRANSLATOR AND MEMORY INTERFACE DEVICE TO TRANSLATE NON-NATAIVE INSTRUCTIONS INTO NATIVE INSTRUCTIONS FOR PROCESSOR (AS AMENDED)

REPLY BRIEF

Mail Stop Reply Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Reply Brief is filed under 37 CFR. §41.41(a)(1) in response to the Examiner's Answer dated November 17, 2006 (hereinafter "Answer"). All arguments contained in the Principal Brief are reasserted herein. The following commentary focuses on the portions of the Answer that respond to the Principal Brief, and the new ground of the rejection of claims 6, 12, and 18.

I. Status of Claims

Claims 1-4, 6-10, 12-16, and 18 remain on appeal. Appellant acknowledges, with appreciation, the Answer's indication in paragraph 25 of pages 15-16 that claims 5, 11, and 17 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

II. Grounds Of Rejection To Be Reviewed

A. Claims 1, 7, and 13 stand rejected as being anticipated by U.S. Patent 6,292,883 ("Augusteijn") under 35 U.S.C. §102(e).

B. Claims 2-4, 8-10, and 14-16 stand rejected as being unpatentable over Augusteijn in view of IBM Technical Disclosure Bulletin, NN610843 ("IBM TDB") under 35 U.S.C. §103(a).

C. Claims 6, 12, and 18 stand rejected as being unpatentable over Augusteijn in view of U.S. Patent 5,386,547 ("Jouppi") under 35 U.S.C. §103(a).

III. Argument

A. Rejection of claims 1, 7, and 13 under 35 U.S.C. §102(e) by Augusteijn

Claim 1 recites, among other things,

> a select circuit for selectively applying the information read from said external memory space and the instruction prepared by translating the instruction read from said external memory space by said translator to said processor core depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not.

The claimed invention provides the information (including a nonnative instruction, a native instruction and data), or the instruction translated from the nonnative instruction, to the processor core depending on where such information or instruction is fetched from.

The Answer, stated in paragraph 22 bridging pages 12-14, reads the claimed select circuit on the combination of detector 440 and feeder 136 in Fig. 4 of Augusteijn, as reproduced below (emphasis added):

> Augusteijn disclosed the claimed limitation through the combination of elements 440 and 136 from figure 4. Element 440 is a detector element that is able to determine if the incoming instruction is an instruction that needs no translation and can be sent directly to element 136 (Column 10, lines 45-56). The incoming instruction comes from external memory element 120 from figure 1. The external memory is divided up into several sub ranges for storing either instructions that need to be translated or instructions that don't need to be translated (Column 10 lines 45-56). Thus, detector 440 is able to determine if the incoming instruction is to be translated or not by looking at where the instruction originated from in memory (Column 10 lines 45-56). Element 136 is then able to receive either a native instruction to the processor via element 440 or a translated instruction via elements 400, 410, or 420. Element 136 then selects from the appropriate line to send to the execution unit depending on the instruction being translated or not (Column 10 lines 45-56). Thus, elements 136 and 440 read upon the limitation with element 136 selecting a native instruction from an external memory 120 or selecting a translated instruction from elements 400, 410, or 420 and sending the instruction to the processor depending on the region of memory the instruction is in, which is determined by element 440.

Appellant submits that Augusteijn does not disclose, and the Answer does not explain where Augusteijn describes, "selectively applying the information read from said external

memory space and the instruction prepared by the translation of the instruction... to said processor core depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not."

Even if it were to be assumed that Augusteijn discloses that detector 440 is able to determine if the incoming instruction is to be translated or not by looking at where the instruction originated from in memory for the sake of this Brief, Augusteijn does ***not*** describe, at a minimum, that detector 440 is configured for selectively ***applying*** the instruction from an external memory space and the ***instruction converted*** by conversion means 400, 410, or 420 ***to a processor core*** based on an address value. As asserted in the Answer, detector 440 is configured to detect whether or not conversion of an instruction is required (native instruction need not be converted) and which conversion means should be used for the conversion (see column 6, lines 4-8 of Augusteijn et al.). Detector 440 is ***not*** configured to ***select*** a non-converted instruction or a ***converted instruction***, and apply a selected instruction to microprocessor core 114. Therefore, the claimed select circuit is distinguishable from the detector 440 of Augusteijn.

With respect to feeder 136, the Answer asserted that "Element 136 then selects from the appropriate line to send to the execution unit depending on the instruction being translated or not." Although Appellant takes issue with assertion, for the sake of this Brief, Augusteijn does not disclose, and the Answer did not point out where Augusteijn discloses, that feeder 136 is configured to select a non-converted instruction or a converted instruction, and apply the selected one to microprocessor core 114 ***based on whether an address value for access from microcontroller core 114 to the external memory space is in a predetermined region or not***. Rather, Augusteijn simply describes, "The pre-processor 130 further comprises a feeding means 136 for feeding native instructions of the sequence to the microcontroller core 114 for execution"

(column 7, lines 28-29); and "If also native instructions are stored in the instruction memory 120, the detector 440 ensures that these instructions are directly supplied to the feeder 136 for supply to the microcontroller core 114" (column 10, lines 53-56). Accordingly, feeder 136 is not configured to selectively applying instructions to microprocessor core 114 based on an address value.

Consideration of the teachings of detector 440 and feeder 136 would not have suggested, among other things, "selectively applying the information read from said external memory space and the instruction prepared by the translation of the instruction read from said external memory space to said processor core depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not," as recited in claim 1. As Augusteijn has no disclosure of the "select circuit" of claim 1, Augusteijn fails as an anticipatory reference for claim 1.

The above discussion is applicable to claims 7 and 13. It is submitted that Augusteijn also fails as an anticipatory reference for claims 7 and 13.

B. Rejection of claims 2-4, 8-10, and 14-16 under 35 U.S.C. §103(a) over Augusteijn in view of IBM TDB

Neither Augusteijn nor IBM TDB discloses the additional requirements recited in the claims, nor have they been addressed in the Office Action. Specifically, IBM TDB does not teach, among other things, a processor having a native operation mode with data stored in memory at twice the size of a non-native operation mode, as asserted in the Office Action. Moreover, the IBM TDB disclosure does not cure the argued fundamental deficiencies of Augusteijn with respect to the rejection of parent claim 1 under 35 U.S.C. §102(e).

It is submitted, therefore, that the rejection of claims 2-4, 8-10 and 14-16 fails both for the lack of disclosure in the applied references of all requirements of parent claims 1, 7 and 13, and for the additionally recited elements.

C. Rejection of claims 6, 12, and 18 under 35 U.S.C. §103(a) over Augusteijn in view of Jouppi

This is the new ground of rejection introduced by the Answer.

Claim 6 is dependent from claim 1 and additionally requires as follows:

> said processor core has an instruction bus, an instruction address bus, a data bus and a data address bus, and
>
> said data processing device further includes:
>
> a multiplexer having inputs connected to said instruction address bus and said data address bus, respectively, for selecting said instruction address bus or said data address bus for application to said fetch circuit in response to the control signal applied from said processor core, and
>
> a second multiplexer for electrically coupling said memory bus to said instruction bus or said data bus, in response to said control signal applied from said processor core.

Claims 12 and 18 contain similar requirements.

The applied combination of Augusteijn and Jouppi does not teach a data processing device including all the limitations recited in parent claim 1 upon which claim 6 depends. The additional comments in the Answer and citation of Jouppi do not cure the argued fundamental deficiencies of Augusteijn with respect to the rejection of parent claim 1 under 35 U.S.C. §102(e).

Accordingly, claim 6 is patentably distinguishable over Augusteijn and Jouppi at least because the claim includes all the limitations recited in parent claim 1.

It is submitted, therefore, that the rejection of claims 6, 12, and 18 fails at least for the lack of disclosure in the applied references of all requirements of parent claims 1, 7 and 13.

IV. Conclusion

For all of the foregoing reason, Appellant respectfully submits that none of rejections of record is legally viable. Reversal of all rejections is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Tomoki Tanida
Limited Recognition No. L0098

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 SAB:TT
Facsimile: 202.756.8087
Date: January 17, 2007

Please recognize our Customer No. 20277 as our correspondence address.

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